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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/478,714	01/06/2000	TONY S. EL-KIK	BAYS-10-8-2	2054

8933 7590 10/19/2004

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/478,714	EL-KIK ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 17-23 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 9/3/04.

Claim Objections

3. Claim 1 is objected to because of the following informalities: In line 2, insert a comma after "signals". Also, in the first line of part (b), insert a comma after "data bus". Appropriate correction is required.

4. Claim 20 is objected to because of the following informalities: In line 2, insert a comma after "signals". Also, in the first line of part (b), insert a comma after "data bus". Appropriate correction is required.

Withdrawn Rejections

5. Due to the cancellation of the claims rejected in the previous Office Action, the rejections of those claims are hereby withdrawn. However, a new ground(s) of rejection is applied to the newly added claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 17-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Campanini, U.S. Patent No. 4,700,292 (as applied in the previous Office Action).

7. Referring to claim 17, Campanini has taught a dual processor system, comprising:

a) a first processor having one address bus, one data bus, control signals, and memory accessible via the address bus and data bus. See column 4, lines 25-27, and Fig.1. Note that component EL_A is a processor comprising memory and it has a bus B_C which is an address bus, a data bus, and a control signal bus. This is evident in Fig.4 where it is shown that bus B_C passes control signals RD, RY, WR, and AK. Also, data and addresses are passed along this bus to a second processor in order to allow for burst transfer. See column 7, lines 23-32, column 3, lines 29-43, claim 1, and the abstract, for examples of this.

b) a second processor coupled directly to the address bus, data bus, and control signals of said first processor, the second processor comprising a control register with a control register system address, an internal memory (Fig.1, components DIS_B and MED_B), a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory. See column 4, lines 25-27, and Fig.1, component EL_B. Note this processor is connected directly to processor EL_A via bus B_C. In addition, note the control register comprises the MEA and WCA storage locations in Fig.5. Both

of these locations control the second processor during transfer mode. Also, note that these registers are read from and written to for increment and decrement purposes, respectively (see column 9, lines 27-34). Therefore, in order to read and write to specific locations, the control registers must be addressable. Furthermore, see Fig.4, and note the REI register. This data register receives all incoming words where the words are then propagated to the buffer store (FIFO) and ultimately, to the appropriate destination within the internal memory. Also, note that the WR signal, which indicates a write is going to occur, is used to specify a word is being transferred. See column 9, lines 27-34. Therefore, the WR signal will act as a system address for the data register in that it results in the data register receiving some data. Note also that this data register is coupled to the internal memory since the internal memory is the final destination for the transferred words. Finally, see column 9, lines 26-34 for teachings of an internal address generator. Note that the MEA control register initially holds the starting internal memory address. This address is incremented by an internal address generator each time a new word is being transferred to memory.

c) wherein the first processor can read from and write to the internal memory of the second processor by:

c1) placing a control word on the first processor data bus and asserting the first processor address bus and control signals to select the control register of the second processor, said control word containing a starting address from which the second processor reads from or writes to said internal memory. Note that header data is sent prior to the actual data words that are to be transferred. See the abstract. This header includes the number of words to be transferred and the starting destination address. See column 2, lines 33-38,

and column 8, line 61, to column 9, line 10. Note that the control register is addressed appropriately, such that the word count is put in the WCA control register and the starting address is put in the MEA register. Addresses need to be provided in order to select one of these registers.

c2) the second processor, without receiving a data word count or stop address from the first processor, enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting address and incrementing upward during subsequent data transfer cycles, so long as the first processor asserts the data register system address on its address bus. See column 9, lines 24-38. As long as the counter is greater than zero and was initially greater than one, burst mode is indicated, and data words will be transferred. A stop address is not received by the second processor from the first processor. Instead, a starting address is received and the value of the counter (number of words to be transferred) determines what the stop address will be. For each count of the counter, the starting address is incremented. For instance, a write burst mode is taught in column 9, lines 24-38. Basically, the first processor asserts the WR signal, specifying a write to the data register and then transfers the data word to be written. This word will then be stored at the address specified by the MEA register (which was set by the control word), where the value of this register is incremented for as many words that are to be transferred, which is specified by the WCA register (also set by the control word). Furthermore, a read burst mode is taught in column 9, lines 24-38, and column 1, lines 7-10, where it is shown that the relationship between processors is interchangeable, i.e., the first processor can be the sender or the

receiver. In this situation, when the first processor is to receive from the slave, this would be read mode, and it would work much like the write mode mentioned above.

8. Referring to claim 18, Campanini has taught a dual processor system as described in claim 17. Campanini has further taught:

a) in a write burst mode, following the transmission of said control word, the first processor asserts the data register system address on the first processor address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting address, whereby the subsequent data words are written into the consecutive memory locations until the first processor ceases to assert the data register system address. See column 9, lines 24-38, for disclosure regarding a write burst mode. Basically, the first processor asserts the WR signal, specifying a write to the data register and then transfers the data word to be written. This word will then be stored at the address specified by the MEA register, where the value of this register is incremented for as many words that are to be transferred, which is specified by the WCA register. And, it should be realized that the writing would continue as long as the first processor has something to write, i.e. something to write to the incoming register of the second processor.

b) wherein, in a read burst mode, following the transmission of said control word, the first processor asserts the data register system address on the first processor address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting address, and the second processor clocks data words at the consecutive memory locations into the data register and places said data words on the data bus, whereby the subsequent data words are read from the

consecutive memory locations by the first processor through the data register until the first processor ceases to assert the data register system address. A read burst mode is taught in column 9, lines 24-38, and column 1, lines 7-10, where it is shown that the relationship between processors is interchangeable, i.e., the first processor can be the sender or the receiver. In this situation, when the first processor is to receive from the slave, this would be read mode, and it would work much like the write mode mentioned above in reverse.

9. Referring to claim 19, Campanini has taught a dual processor system as described in claim 17. Campanini has further taught that said control signals comprise at least a read and a write signal. See Fig.4 and note the control signals WR and RD.

10. Referring to claim 20, it has been noted by the examiner that the only difference between claim 17 and claim 20 is that claim 17 claims a dual processor system while claim 20 claims a multiprocessor system. However, a dual-processor system is a multi-processor system. Consequently, claim 20 is rejected for the same reasons set forth in the rejection of claim 20. It should be realized that if more than two processors existed and a main processor is to communicate with only one of the multiple coprocessors at any given time, then a unique address associated with the specific coprocessor must be presented.

11. Referring to claim 21, Campanini has taught a multi-processor system as described in claim 20. Furthermore, it has been noted by the examiner that the only difference between claim 18 and claim 21 is that claim 18 claims a dual processor system while claim 21 claims a multiprocessor system. However, a dual-processor system is a multi-processor system. Consequently, claim 21 is rejected for the same reasons set forth in the rejection of claim 18.

12. Referring to claim 22, it has been noted that the system of claim 17 include a second processor which performs the same functions as the coprocessor of claim 22. Consequently, claim 22 is rejected for the same reasons set forth in claim 17.

13. Referring to claim 23, Campanini has taught a dual processor system as described in claim 17. Campanini has further taught that the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, and the data is transferred from the first processor to a specified location into memory of the second processor during the next data transfer cycle when the control word has a burst mode bit that does not indicate burst mode. Recall that header data is sent prior to the actual data words that are to be transferred. See the abstract. This header includes a control word, which includes the number of words to be transferred and the starting destination address. See column 2, lines 33-38, and column 8, line 61, to column 9, line 10. Note that the control register is addressed appropriately, such that the word count is put in the WCA control register and the starting address is put in the MEA register. Addresses need to be provided in order to select one of these registers. Note that the word count, stored in the WCA register, includes a burst mode indication. If the word count is stored as an X-bit number, then the X-1 most significant bits are the burst mode indicators. If any one of those bits is set to 1, then that bit is a burst mode bit. This can be seen with a simple example. Suppose, one word is to be transferred (non-burst mode) and the word count is appropriately set to 00000001 (where X=8). The seven (X-1) most significant bits are set to 0, indicating that the processors are not in burst transfer mode. However, if three words were to be transferred and the word count were set to 00000011, then it can be seen that one of the seven most significant bits is set to 1, indicating

burst mode. Therefore, that bit would be a burst mode bit. If burst mode is not indicated, only a single word would be transferred, as the count would be equal to 1 and after one word is transferred, the counter will be decremented. Since it will equal 0, data transfer is finished. The process is generally described in column 9, lines 24-28.

Response to Arguments

14. Applicant's arguments filed on September 3, 2004, have been fully considered but they are not persuasive.

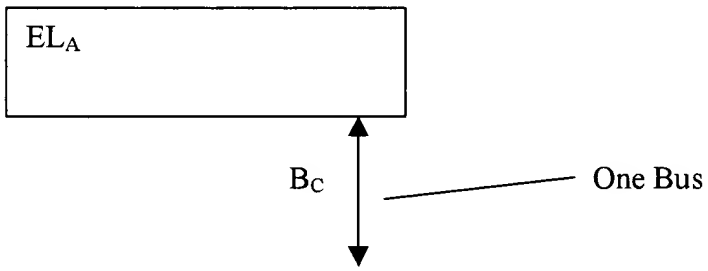
15. Applicant argues the novelty/rejection of claim 17 on pages 7-8 of the remarks, in substance that:

> "The prior art of record neither discloses nor suggests "a first processor having one address bus, one data bus, control signals and memory accessible via the address bus and data bus [and] a second processor coupled directly to the address bus, data bus and control signals of said first processor" Instead, the reference (Campanini) shows a two-processor system wherein the processors each have their own internal address and data buses as well as interface hardware for communications over yet a third bus.
>
> Referring to Figure 1 in Campanini, both central processing units (CPUA and CPUB) communicate over their individual internal buses (BA and Bs) with a dedicated interface (INTA and INDB). The interfaces are what connect the dual processors over yet a third bus (Bc). Unlike the topography in Campanini, which requires inter-processor communication over a dedicated bus (Bc), claim 17 requires "A dual processor system, comprising: (a) a first processor having one address bus, one data bus, control signals and memory accessible via the address bus and data bus; (b) a second processor coupled directly to the address bus, data bus and control signals of said first processor." (Claim 17)"

16. These arguments are not found persuasive for the following reasons:

a) Applicant refers to processors CPU_A and CPU_B as having their own buses and then having to use a third bus to communicate with one another. However, as the examiner pointed in the previous rejection, components EL_A and EL_B of Fig.1 are each processors which contain the aforementioned CPUs and other components. This is also confirmed in column 4, lines 25-27. When looking at Fig.1, it can be seen that the first processor EL_A has one bus B_C for transmitting

data, addresses, and control signals to the second processor EL_B. Clearly, from the figure, the second processor is coupled directly to that bus. Applicant is correct in saying that each has its own internal bus but the processor as a whole has one bus, thereby anticipating applicant's claimed one bus. In addition, with applicant's use of the word "comprising" the claim is open, wherein the prior art may contain additional elements and still read on applicant's claims. Just looking at the processor as a whole, this "one bus" concept is more easily seen.



Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
October 14, 2004

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